What is claimed is:

1. A system comprising:

a locked loop circuit; and

a processor coupled to the locked loop circuit to control the locked loop circuit and perform at least one other function in the system not related to the control of the locked loop circuit.

2. The system of claim 1, wherein the locked loop circuit comprises a delay locked loop circuit.

3. The system of claim 1, wherein the locked loop circuit comprises:

an interface accessible by the processor.

4. The system of claim 3, wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit.

5. The system of claim 3, wherein the system comprises a computer system having a system memory and the interface is addressable in a range of addresses used to access the system memory.

6. The system of claim 3, wherein the interface indicates storage accessible by the processor to store an indication of a delay used by the locked loop circuit.

7. The system of claim 3, wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

8. The system of claim 1, wherein the processor comprises a microprocessor.

9. The system of claim 1, further comprising:

a system memory storing a program,

wherein the processor executes the program to perform said other function.

10. A locked loop circuit comprising:

a delay line to receive an input clock signal and furnish an output clock signal;

a phase detector to indicate a phase difference between the input clock signal and the output clock signal; and

an interface accessible by a processor to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal.

11. The locked loop circuit of claim 10, wherein the locked loop circuit comprises a delay locked loop circuit.

12. The locked loop circuit of claim 10, wherein the interface indicates a phase difference between an incoming clock signal to the locked loop circuit and another signal generated by the locked loop circuit.

13. The locked loop circuit of claim 10, wherein the interface is addressable in a range of addresses used to access a system memory of a computer system.

14. The locked loop circuit of claim 10, wherein the interface includes storage accessible by the processor to store an indication of a delay applied by the locked loop circuit to the input clock signal.

15. The locked loop circuit of claim 10, wherein the interface includes storage accessible by the processor to store an indication of a selection of one of a plurality of output clock signals furnished by the locked loop circuit.

16. A method comprising:

providing a locked loop circuit having a processor accessible interface; and

using a processor to control the locked loop circuit and perform at least one other function not related to the control of the locked loop circuit.

17. The method of claim 16, wherein the locked loop circuit comprises a delay locked loop circuit.

18. The method of claim 16, further comprising:

performing at least one of read and write operations to the interface to control the locked loop circuit.

19. The method of claim 16, further comprising:

using the interface to indicate a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit.

20. The method of claim 16, wherein the system comprises a computer system having a system memory and the interface is addressable in a range of addresses used to access the system memory.

21. The method of claim 16, further comprising:

using the interface to store an indication of a delay used by the locked loop circuit.

22. The method of claim 16, further comprising:

using the interface to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

23. The method of claim 16, wherein the processor comprises a microprocessor.